

REVISIONS					
REV	ECN#	ZONE	DESCRIPTION	NAME	DATE
C	----	----	CHANGE AS PER CP121273	D. ACEVAL	10/15/2012
D	----	----	CHANGE AS PER CP121660	V. VADUVA	12/10/2012

NOTE:
1. 1. DUT PIN 17 AND 20 ARE INTERNALLY CONNECTED TO GND PADDLE

D

D

C

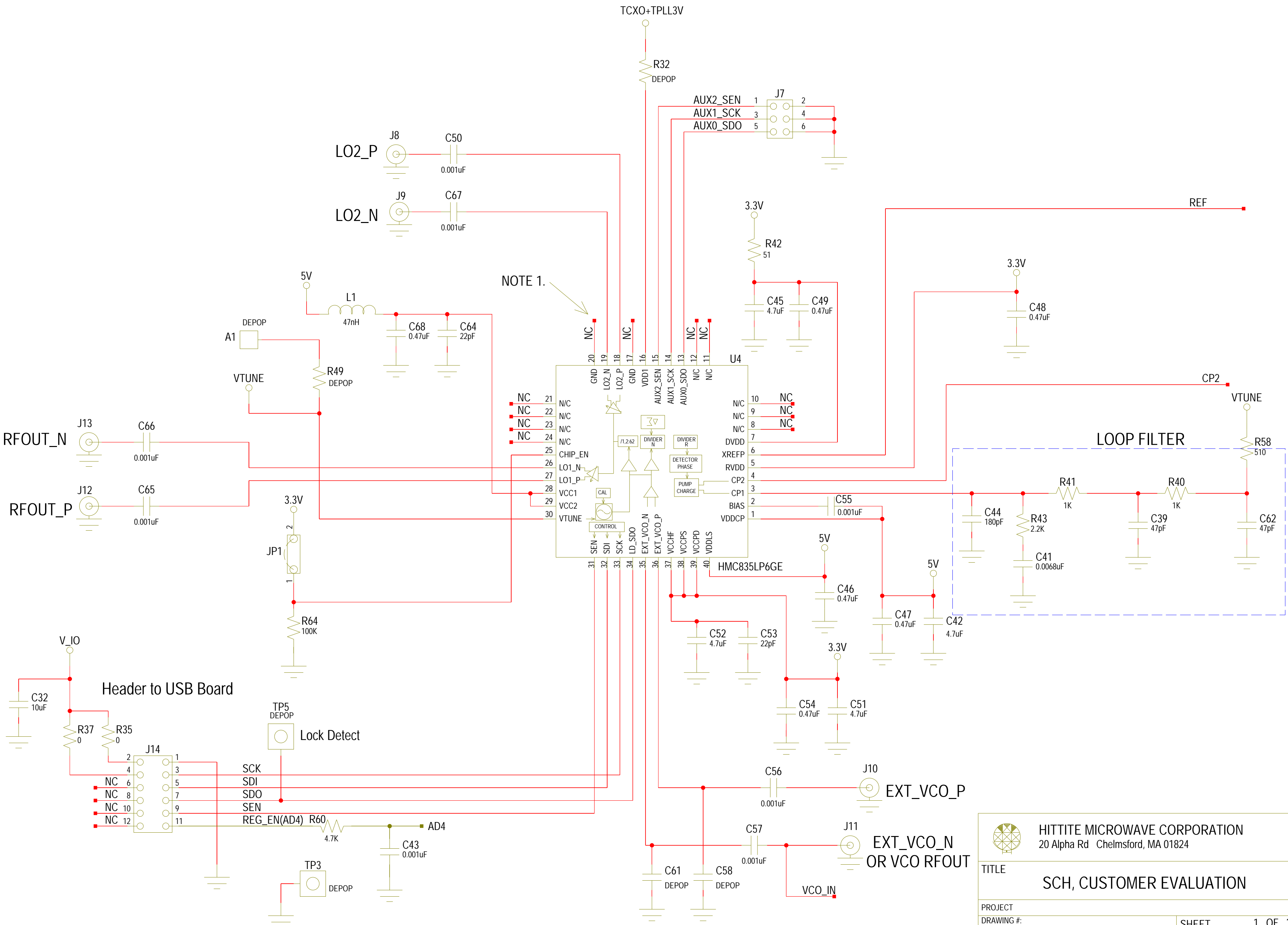
C

B

B

A

A



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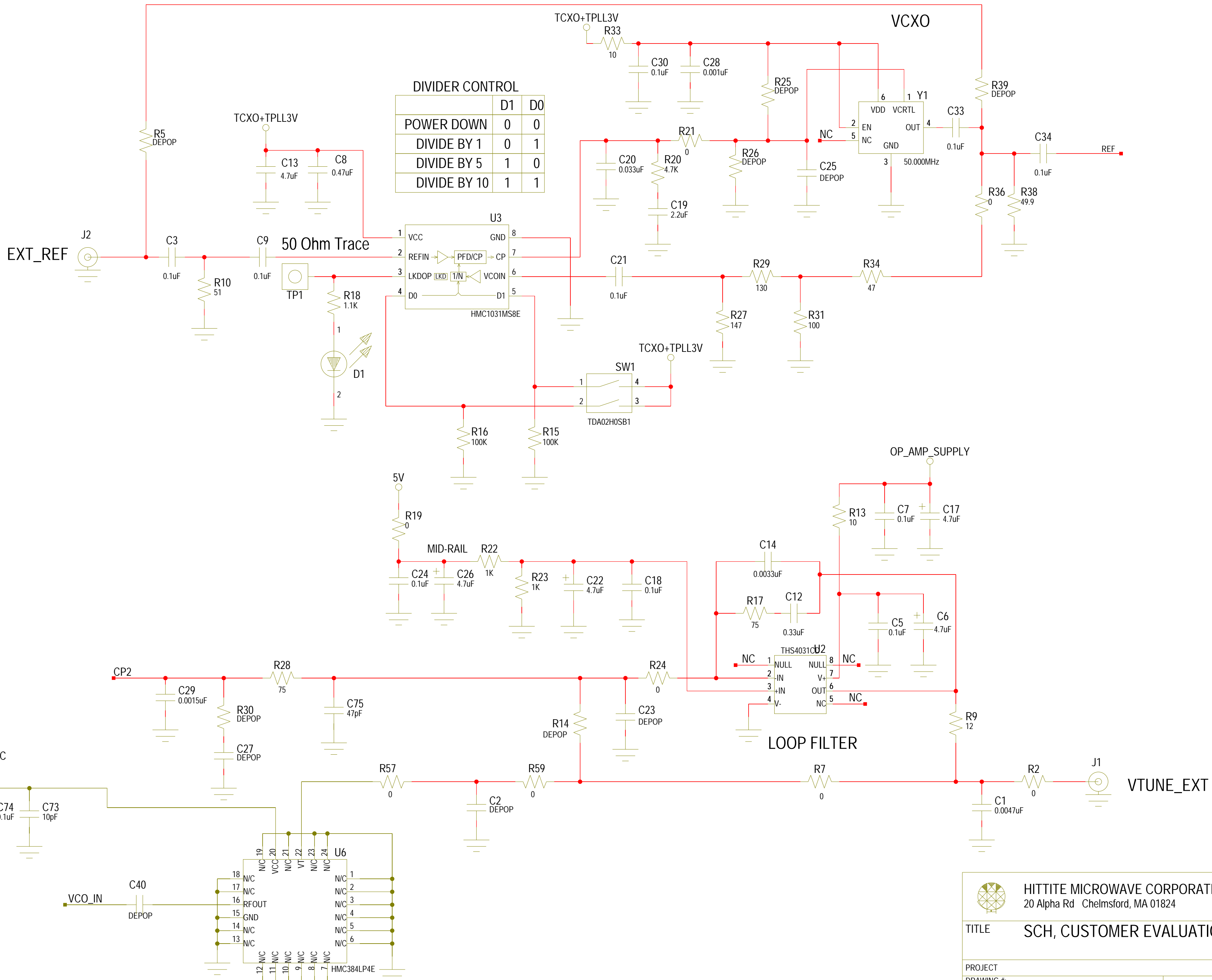
TITLE
SCH, CUSTOMER EVALUATION

PROJECT
DRAWING #: 130-00378-00

SHEET 1 OF 3

DRAWN BY D.YOUNG **DATE** 01/01/2010

CODE ID NO. 1CN88 **SIZE** C **REV** D



DIVIDER CONTROL

	D1	D0
POWER DOWN	0	0
DIVIDE BY 1	0	1
DIVIDE BY 5	1	0
DIVIDE BY 10	1	1

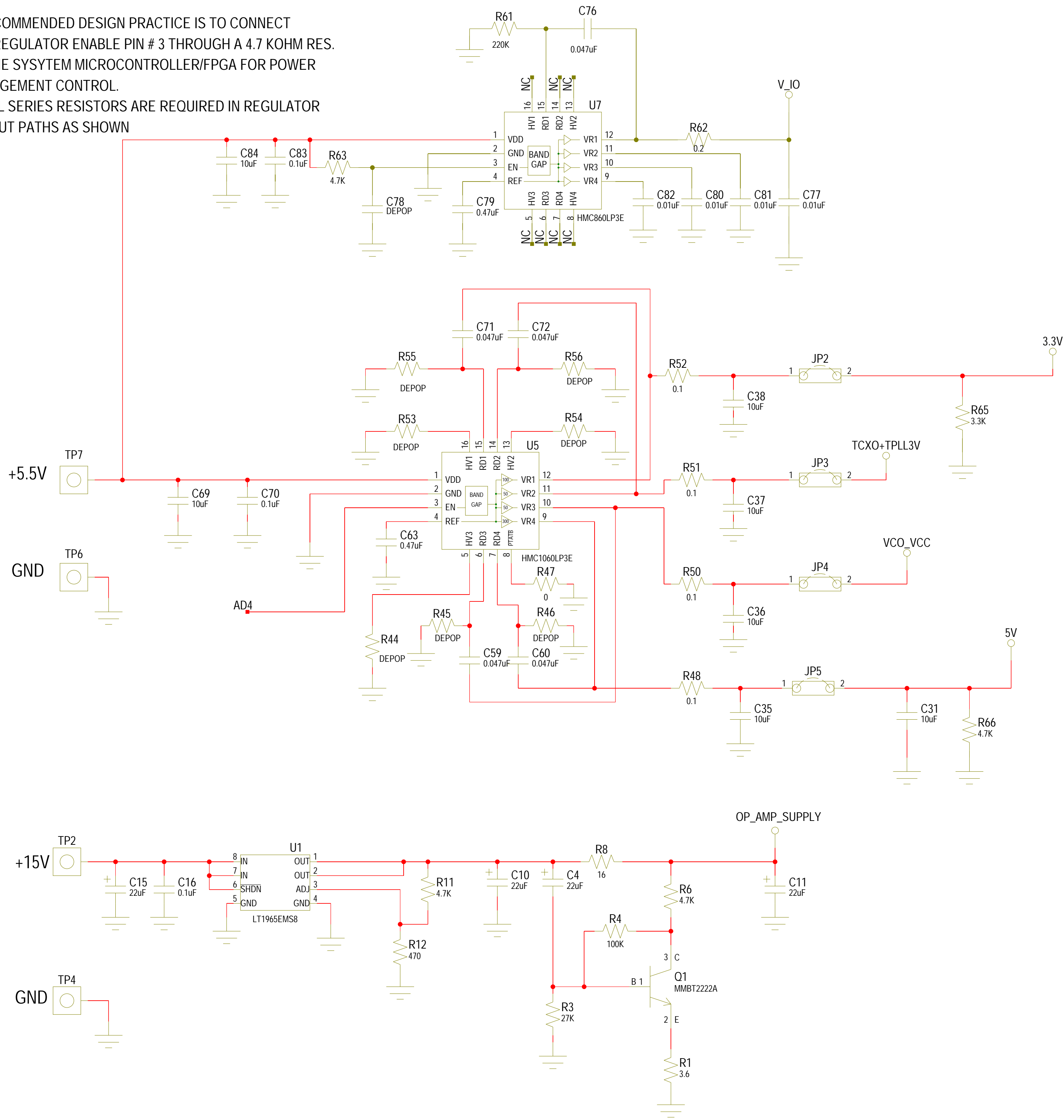
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TITLE **SCH, CUSTOMER EVALUATION**

PROJECT
 DRAWING #: **130-00378-00** SHEET **2 OF 3**

DRAWN BY **D.YOUNG** DATE **01/01/2010** CODE ID NO. **1CN88** SIZE **C** REV **D**

A RECOMMENDED DESIGN PRACTICE IS TO CONNECT THE REGULATOR ENABLE PIN # 3 THROUGH A 4.7 KOHM RES. TO THE SYSTEM MICROCONTROLLER/FPGA FOR POWER MANAGEMENT CONTROL. SMALL SERIES RESISTORS ARE REQUIRED IN REGULATOR OUTPUT PATHS AS SHOWN



 HITTITE MICROWAVE CORPORATION 20 Alpha Rd Chelmsford, MA 01824				
TITLE SCH, CUSTOMER EVALUATION				
PROJECT DRAWING #: 130-00378-00		SHEET 3 OF 3 <small>CODE ID NO. SIZE REV</small>		
DRAWN BY: D.YOUNG	DATE: 01/01/2010	1CN88	C	D